IN THE CLAIMS:

Please amend the claims as follows:

1-20. (**Canceled**)

21. (**Currently Amended**) A memory circuit requiring refresh operations, comprising;

a memory core having memory cells;

a memory control circuit which, for M external operation cycles, where M is greater than or equal to 2 [[(M≥2)]], has N internal operation cycles, where N is greater than M and less than 2M ~~(M<N<2M)~~; and

a refresh command generation circuit which generates refresh commands; and wherein

said N internal operation cycles includes first internal operation cycles which execute external commands corresponding to said external operation cycles, and second internal operation cycles which execute said refresh commands, and

said refresh command generation circuit generates said refresh commands according to a reception of said external command.

22. (**Original**) The memory circuit according to claim 21, wherein the frequency of said external clock signal is higher than the frequency of said external operation cycles;

further comprising an internal clock generation circuit which generates an internal clock signal defining said internal operation cycles according to the external clock signal; and,

said external commands are supplied according to a cycle which is equal to or greater than said external operation cycle, and are input in synchronization with said external clock signal.

23. (**Original**) The memory circuit according to claim 22, wherein said refresh command generation circuit permits the generation of said refresh commands according to the combination of external commands, which are input in synchronization with a prescribed number of said external clock cycles.

24. (**Original**) The memory circuit according to claim 22, wherein said refresh command generation circuit permits the generation of said refresh commands when said external commands are not input in synchronization with any of the external clock cycles among a prescribed number of said consecutive external clock cycles.

25. (**Original**) The memory circuit according to claim 22, wherein in cases where the frequency of said external commands is L times the frequency of said external operation cycles, said refresh command generation circuit permits the generation of said refresh commands when said external commands are not input in synchronization with any of (L-1) external clock cycles among said L consecutive external clock cycles, and within said M external operation cycles, combinations of said (L-1) external clock cycles are circulated.

26. (**Original**) The memory circuit according to claim 22, wherein in cases where the frequency of said external commands is L times the frequency of said external operation cycles,

further comprising:

an internal command register which holds said external commands in the most recent L external clock cycles, and generates corresponding internal commands according to the held external commands; and wherein

in prescribed cycles among said N internal operation cycles, said internal command register ignores the held external commands in some cycles among said L held external commands, and generates said internal commands.

27. (**Original**) The memory circuit according to claim 26, wherein said refresh command generation circuit permits generation of said refresh commands according to internal commands generated by said internal command register.

28. (**Original**) The memory circuit according to claim 26, wherein said refresh command generation circuit permits the generation of said refresh commands when there exist no internal commands generated by said internal command register.

29. (**Currently Amended**) The memory circuit according to any one of claims 23 through 28, wherein said refresh command generation circuit generates said refresh commands during a state of permission of said refresh command generation, in response to generation of refresh timer signals generated with prescribed timing.

30-45. (**Canceled**)